

AMENDMENTS TO THE CLAIMS

Please amend prior claims 19 and 25 as indicated below, and add new claims 34 and 35. In accordance with 37 C.F.R. § 1.121, a claim listing including the status and text of all claims as currently presented appears below. In making such amendments, no new matter is entered.

1. (Withdrawn) A method for manufacturing multi-layered electronic devices, said method comprising the steps of:

providing a first device layer with a first series of resistive/conductive patterns thereon;

providing a second device layer with a plurality of via drilled therethrough; bonding said first and said second device layers together to form a unitary body, wherein each of said via correspond to a respective capture pad in said first series of resistive/conductive patterns;

providing a second series of resistive/conductive patterns on an outer layer of said unitary body;

providing a plurality of terminations on said unitary body for electrical connection to other electronic devices;

inserting individual passive components vertically into each of said plurality of via;

bonding each of said passive components to its respective capture pad; filling said via with a non-conductive material; and

forming electrical connections between each of said passive components and at least a portion of said second resistive/conductive patterns on said outer surface of said unitary device body.

2. (Withdrawn) The method of claim 1, wherein said first and said second device layers are made of FR4.

3. (Withdrawn) The method of claim 2, wherein said device is a printed circuit board.

4. (Withdrawn) The method of claim 1, wherein said first and second device layers are made of a non-conductive ceramic.

5. (Withdrawn) The method of claim 4, wherein said device is an integrated passive device.

6. (Withdrawn) The method of either claim 3 or 4, wherein the method of bonding said first and said second device layers is selected from the group consisting of: lamination, weight-firing, gluing or spritzing solvent.

7. (Withdrawn) The method of claim 1, further comprising, prior to providing said plurality of terminations, the steps of:

firing said device body to cure said second series of resistive/conductive patterns; and

trimming said second series of resistive/conductive patterns to achieve predefined component values.

8. (Withdrawn) The method of claim 1, wherein said passive components comprise any combination of resistors capacitors, varistors, and thermistors.

9. (Withdrawn) The method of claim 8, wherein said passive components are bonded to their respective capture pads by way of solder reflow.

10. (Withdrawn) The method of claim 8, wherein said passive components are bonded to their respective capture pads by way of cured conductive epoxy.

11. (Withdrawn) The method of manufacturing multi-layer electronic devices, said method comprising the steps of:

providing a first device layer with at least one ground plane thereon;

providing a second device layer with a plurality of via drilled therethrough;

bonding said first and said second device layers together to form a unitary body, wherein each of said via correspond to a respective capture pad in electrical connection with said at least one ground plane;

providing a series of resistive/conductive patterns on an outer layer of said unitary body;

providing a plurality of terminations on said unitary body for electrical connection to other electronic devices, said at least one ground plane being in electrical communication with at least one of said terminations;

inserting individual passive components vertically into each of said plurality of via;

bonding each of said passive components to its respective capture pad; and

forming upper lands between each of said passive components and at least a portion of said resistive/conductive patterns on said outer surface of said unitary device body.

12. (Withdrawn) The method of claim 11, wherein said first and said second device layers are made of FR4.

13. (Withdrawn) The method of claim 12, wherein said device is a printed circuit board.

14. (Withdrawn) The method of claim 11, wherein the method of bonding said first and said second device layers is selected from the group consisting of: lamination, weight-firing, gluing or spritzing solvent.

15. (Withdrawn) The method of claim 11, further comprising, prior to providing said plurality of terminations, the steps of:

firing said device body to cure said second series of resistive/conductive patterns; and

trimming said second series of resistive/conductive patterns to achieve predefined component values.

16. (Withdrawn) The method of claim 11, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

17. (Withdrawn) The method of claim 16, wherein said passive components are bonded to their respective capture pads by way of solder reflow.

18. (Withdrawn) The method of claim 16, wherein said passive components are bonded to their respective capture pads by way of cured conductive epoxy.

19. (Currently Amended) A multi-layer electrical device comprising:

a first device layer with a first series of resistive/conductive patterns thereon;
a second device layer with a plurality of via drilled therethrough;

wherein said first and second device layers comprise an epoxy-fiberglass composite material;

a unitary device body formed by the bonded union of the first and second device layers, wherein said via correspond to a respective capture pad in said first series of resistive/conductive patterns;

a second series of resistive/conductive patterns on an outer layer of said unitary body;

a plurality of terminations on said unitary body for electrical connection between other electronic devices and components of said device;

individual passive components with first and second opposing electrical terminations, wherein each said individual passive component is vertically mounted into a selected of said plurality of via and wherein one of said first and second opposing electrical terminations is bonded to the respective capture pad for said selected of said plurality of via;

multiple portions of a non-conductive material respectively substantially filling the spaces defined by respective vias between each of said individual passive components and the surrounding via said second device layer, wherein said non-conductive material partially encases each said individual passive component to hold it in place while leaving one of said first and second opposing electrical terminations exposed and prevents shorting between respective first and second opposing electrical terminations; and

an electrical connection between each of said passive components and at least a portion of said second series of resistive/conductive patterns on said outer surface of said unitary device body.

20. (Previously Presented) The multi-layer electrical device of claim 19, wherein said first and second layer are made of FR4.

21. (Previously Presented) The multi-layer electrical device of claim 20, wherein said device is a printed circuit board.

22. (Canceled)

23. (Canceled)

24. (Previously Presented) The multi-layer electrical device of claim 19, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

25. (Currently Amended) A multi-layer electronic device comprising:

a plurality of first device layers, each such layer having a first series of resistive/conductive patterns thereon and a plurality of via drilled therethrough;

a plurality of second device layers, each such layer having a plurality of via drilled therethrough;

wherein said first and second device layers comprise an epoxy-fiberglass composite material;

a unitary device body formed by the bonded union of an interleaved stack of said plurality of first and said second device layers, wherein each of said via correspond to a respective portion of the resistive/conductive patterns on the underlying device layer

and wherein one of said second device layers forms the uppermost device layer and the lowermost device layer is one of said first device layers;

 a second series of resistive/conductive patterns on an outer layer of said uppermost device layer;

 a plurality of terminations on said unitary body for electrical connection between other electronic devices and various of the resistive/conductive patterns throughout said unitary device body;

 individual passive components with respective first and second opposing terminations, wherein each individual passive component is vertically mounted into a selected of said plurality of via and wherein one of said first and second opposing terminations are electrically connected to a portion of said underlying first device layer's first series of resistive/conductive patterns;

 multiple portions of a non-conductive material respectively substantially filling the spaces defined by respective vias between each of said individual passive components and ~~the surrounding via~~ said second device layers, wherein said non-conductive material partially encases each said individual passive component to hold it in place while leaving one of said first and second opposing electrical terminations exposed and prevents shorting between respective first and second opposing electrical terminations; and

 an electrical connection between each of said passive components and at least a portion of said overlying first device layer's first series of resistive/conductive patterns through a corresponding one of said first device layer's plurality of via.

26. (Previously Presented) The multi-layer electrical device of claim 19, wherein said bonded union of the first and second device layers is formed of one of lamination, weight-firing, gluing and spritzing solvent.

27. (Previously Presented) The multi-layer electrical device of claim 19, wherein said passive components are bonded to their respective capture pads by way of solder reflow.

28. (Previously Presented) The multi-layer electrical device of claim 19, wherein said passive components are bonded to their respective capture pads by way of cured conductive epoxy.

29. (Previously Presented) The multi-layer electronic device of claim 25, wherein said first and second device layers comprise FR4.

30. (Previously Presented) The multi-layer electronic device of claim 25, wherein said bonded union of the interleaved stack of said plurality of first and said second device layers is formed of one of lamination, weight-firing, gluing and spritzing solvent.

31. (Previously Presented) The multi-layer electronic device of claim 25, wherein said passive components are bonded to their respective capture pads by way of solder reflow.

32. (Previously Presented) The multi-layer electronic device of claim 25, wherein said passive components are bonded to their respective capture pads by way of cured conductive epoxy.

33. (Previously Presented) The multi-layer electronic device of claim 25, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

34. (New) The multi-layer electrical device of claim 19, wherein said multiple portions of non-conductive material comprise insulative epoxy.

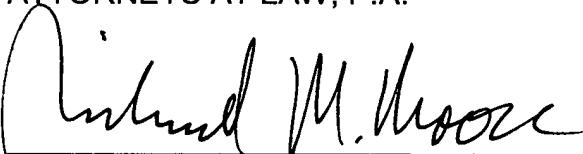
35. (New) The multi-layer electronic device of claim 25, wherein said multiple portions of non-conductive material comprise insulative epoxy.

CONCLUSION:

Inasmuch as all outstanding issues have been addressed, it is respectfully submitted that the present application, including claims 19-21 and 24-35, is in complete condition for issuance of a formal Notice of Allowance, and action to such effect is earnestly solicited. The Examiner is invited to telephone the undersigned at her convenience should only minor issues remain after consideration of this Response in order to permit early resolution of same.

Respectfully submitted,

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